ABSTRACT

A clock delay circuit has a plurality of outputs to provide a sequence of clock signals that togther constitute a multistage clock. The circuit further has a delay adjustment input to adjust the timing of the clock signals for at least one of the outputs relative to the clock signals at another of the outputs. In an embodiment, the circuit has a plurality of these delay adjustment inputs. In a further embodiment, the circuit has a plurality of buffer components to delay the clock signals.